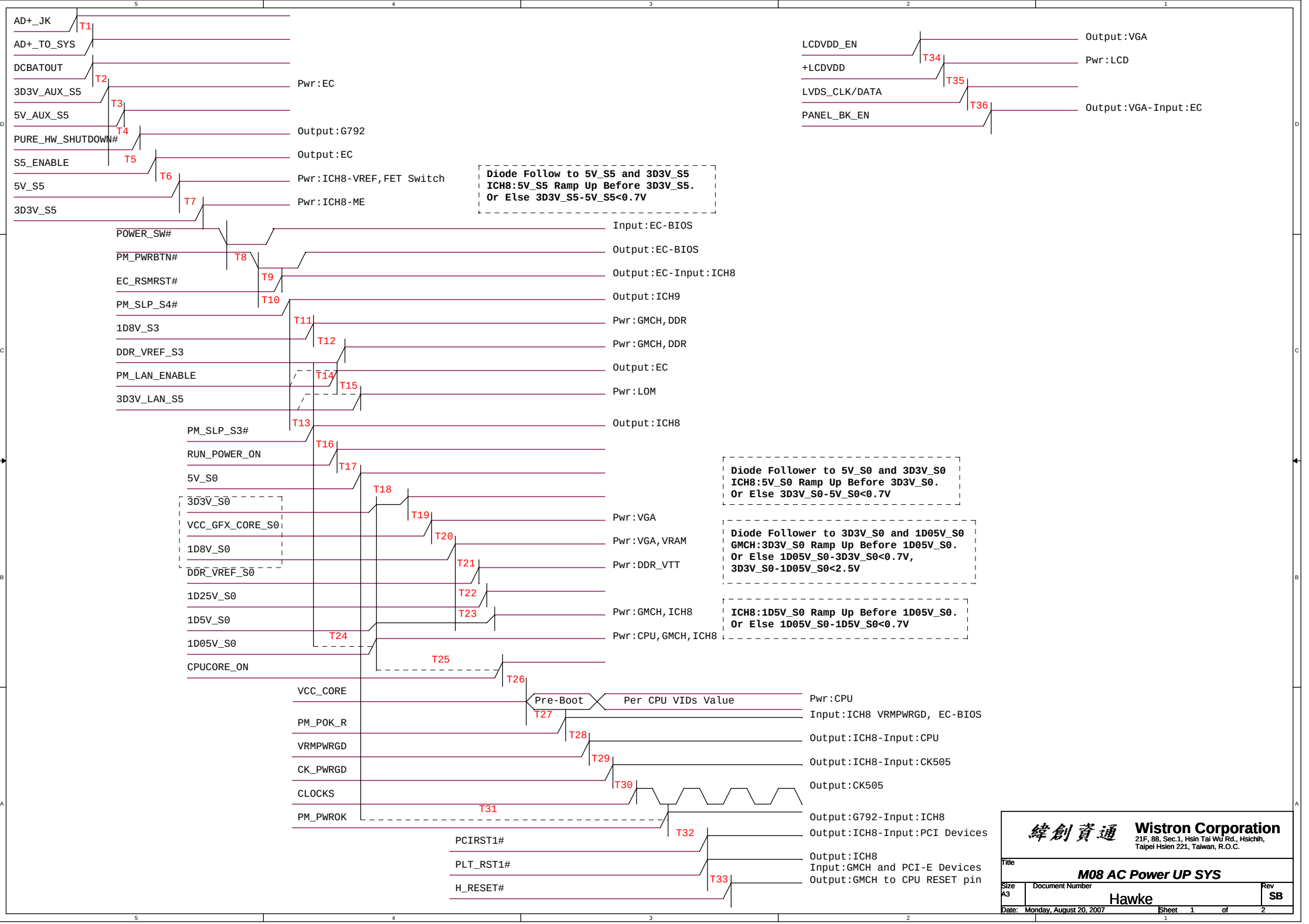
AD+_JK
AD+_TO_SYS
DCBATOUT
3D3V_AUX_S5
5V_AUX_S5
PURE_HW_SHUTDOWN#
S5_ENABLE
5V_S5
3D3V_S5
T1
T2
T3
T4
T5
T6
T7
Pwr:EC
Output:G792
Output:EC
Pwr:ICH8-VREF,FET Switch
Pwr:ICH8-ME
Diode Follow to 5V_S5 and 3D3V_S5
ICH8:5V_S5 Ramp Up Before 3D3V_S5.
Or Else 3D3V_S5-5V_S5<0.7V
LCDVDD_EN
+LCDVDD
LVDS_CLK/DATA
PANEL_BK_EN
T34
T35
T36
Output:VGA
Pwr:LCD
Output:VGA-Input:EC
POWER_SW#
PM_PWRBTN#
EC_RSMRST#
PM_SLP_S4#
1D8V_S3
DDR_VREF_S3
PM_LAN_ENABLE
3D3V_LAN_S5
T8
T9
T10
T11
T12
T14
T15
Input:EC-BIOS
Output:EC-BIOS
Output:EC-Input:ICH8
Output:ICH9
Pwr:GMCH,DDR
Pwr:GMCH,DDR
Output:EC
Pwr:LOM
PM_SLP_S3#
RUN_POWER_ON
5V_S0
3D3V_S0
VCC_GFX_CORE_S0
1D8V_S0
DDR_VREF_S0
1D25V_S0
1D5V_S0
1D05V_S0
CPUCORE_ON
T13
T16
T17
T18
T19
T20
T21
T22
T23
T24
T25
T26
Output:ICH8
Pwr:VGA
Pwr:VGA,VRAM
Pwr:DDR_VTT
Pwr:GMCH,ICH8
Pwr:CPU,GMCH,ICH8
Diode Follower to 5V_S0 and 3D3V_S0
ICH8:5V_S0 Ramp Up Before 3D3V_S0.
Or Else 3D3V_S0-5V_S0<0.7V
Diode Follower to 3D3V_S0 and 1D05V_S0
GMCH:3D3V_S0 Ramp Up Before 1D05V_S0.
Or Else 1D05V_S0-3D3V_S0<0.7V,
3D3V_S0-1D05V_S0<2.5V
ICH8:1D5V_S0 Ramp Up Before 1D05V_S0.
Or Else 1D05V_S0-1D5V_S0<0.7V
VCC_CORE
Pre-Boot
Per CPU VIDs Value
T27
PM_POK_R
VRMPWRGD
CK_PWRGD
CLOCKS
PM_PWROK
T28
T29
T30
T31
Pwr:CPU
Input:ICH8 VRMPWRGD, EC-BIOS
Output:ICH8-Input:CPU
Output:ICH8-Input:CK505
Output:CK505
Output:G792-Input:ICH8
PCIRST1#
PLT_RST1#
H_RESET#
T32
T33
Output:ICH8-Input:PCI Devices
Output:ICH8
Input:GMCH and PCI-E Devices
Output:GMCH to CPU RESET pin
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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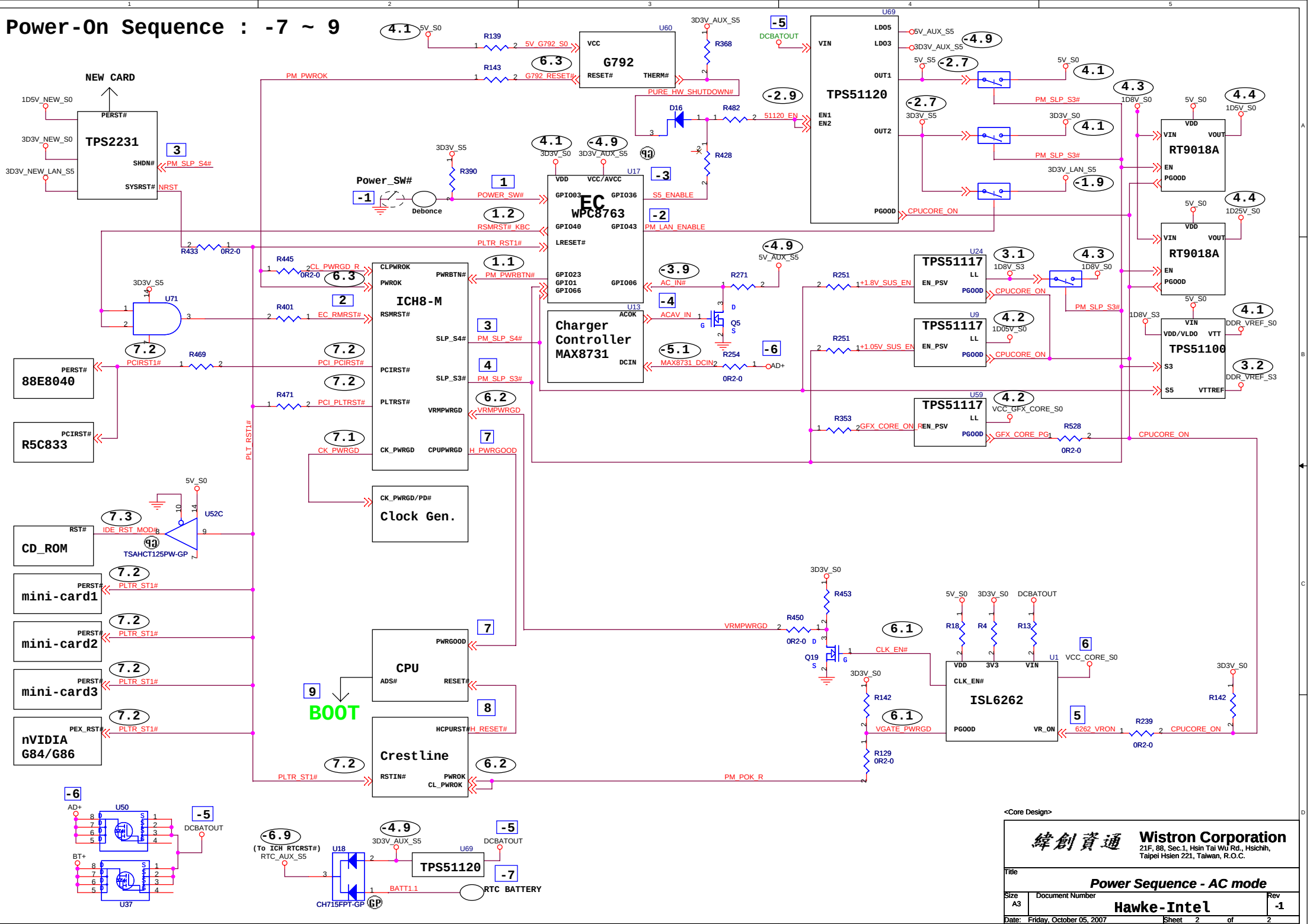
Sheet 1 of 2

Power-On Sequence : -7 ~ 9



<Core Design>

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Title: **Power Sequence - AC mode**

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